Wide-Band VCOs in SiGe Production Technology Operating Up to About 70 GHz

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***Abstract*—Multipurpose VCOs with wide tuning range and oscillation frequencies up to 74 GHz (on wafer) and 69 GHz (mounted chip, with output buffer), respectively, have been fully integrated in a commercial SiGe production technology. To the best of the authors' knowledge these are record values for commercially available Si-based technologies, despite the moderate transistor f_T (62 GHz). The oscillation frequency can easily be dropped down to 41.5 GHz by cutting interconnection lines in the upper metallization layer. The phase noise obtained depends on the frequency range chosen and is sufficiently low for the intended applications.**

***Index Terms*—Millimeter-wave VCO, SiGe bipolar circuit, wide-band VCO.**

I. Introduction

MILLIMETER-WAVE voltage-controlled oscillators (VCOs) are important components in optical-fiber and wireless communication systems. For these applications, LC oscillators in bipolar technologies are preferred to other approaches due to their lower phase noise. Moreover, if transistor operating speed and breakdown voltage are sufficiently high for the intended applications, SiGe should be preferred to InP technologies. For electrical time-division multiplexing (ETDM) in 40-and 80-Gb/s optical-fiber systems, VCOs with low phase noise in the frequency range between 40 to 46 GHz are required. Such circuits can be easily fabricated in today's SiGe production technologies [1]–[3]. However, there are also important applications for VCOs in wireless communications, e.g., at 60 GHz and also at 77 GHz (automotive radar). Therefore, in the present work we tried to find out the frequency limit of a commercial SiGe production technology. Using the same circuit concept and (nearly) the same technology as in [1], [2], the oscillation frequency of the VCO has been increased by more than 20 GHz, mainly by reducing the inductances and capacitances of the resonant circuit. With about 70 GHz, the gap to the 77 GHz application mentioned before is comparatively small and may easily be bridged by applying one of today's preproduction technologies, keeping the basic circuit concept presented here. Moreover, compared to [1], a modified output buffer is used which reliably decouples the oscillator core from the external load and thus allows to mount the chip on a simple and low-cost measurement socket. Finally, it is demonstrated that a wide frequency range can be covered by a single chip without any redesign. For this, only some interconnections in the upper metallization layer have to be interrupted by applying an ultrasonic cutter (used here) or a laser cutter, or by changing a single mask.

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II. Circuit Concept

Fig. 1 shows the simplified circuit diagram of the differential VCO. The oscillator core (which is of the negative-resistance type) and its design has already been discussed in detail in [1], so that we can restrict ourselves to few remarks. All rectangles in Fig. 1 stand for short microstrip-line elements with inductive behavior. The lower of the 4 Cu metallization layers is used as a ground plane for the microstrip lines, thus avoiding substrate losses. The effective lengths of the line elements can be increased (for reducing the oscillation frequency) by cutting bridges between the two complementary lines of the differential microstrip lines, as described in [1], [2]. The MIM capacitor (ΔC_E) shunted to the varactor $(C_{\rm var})$ reduces the oscillation frequency and has to be eliminated at maximum frequencies by cutting the interconnections.

Basically, the oscillator can be used without output buffer if it is loaded by a circuit on the same chip or, possibly, even by another chip directly bonded to the output pads (which are connected to the collector nodes of transistors T) [1], [2]. In this case, the VCO consumes 290 mW at -5.5 V supply voltage. However, if the VCO is mounted in a simple measurement socket an output buffer is required to decouple the oscillator core from the external (nonideal) load [1]. This buffer, shown in Fig. 1, consists of an emitter-follower pair and an emitter-coupled differential stage succeeded by a cascode stage. Loading of the oscillator core by the buffer input is weakened by using an inductive voltage divider (L_{C1}, L_{C2}). The line inductances L_{CQ} are used for output matching. C_P and L_Q represent the output pad capacitance and bond inductance, respectively.

The buffer proved to have an excellent decoupling behavior up to the maximum oscillation frequency (about 69 GHz). However, in the upper frequency ranges of the VCO the gain of the buffer is quite low and its power consumption high (about 460 mW). This is mainly due to the comparatively low transistor

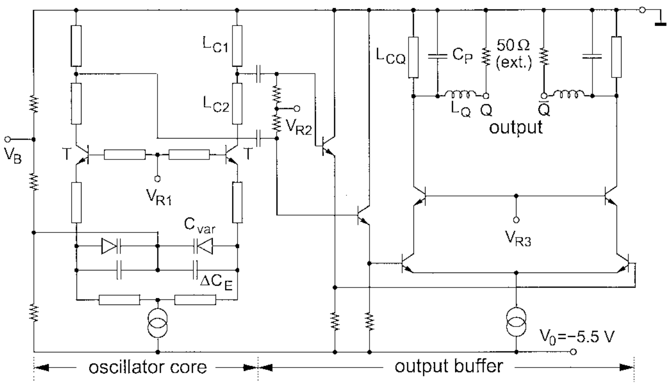

Fig. 1. Circuit diagram of the VCO with output buffer. All reference voltages $V_{Rv}(v = 1\ldots3)$ are generated on chip. Only a single supply voltage is required (V_0). All rectangles represent short adjustable microstrip lines.

f_T (see Section III).[1] In the lower frequency ranges (e.g., below 50 GHz), power consumption could be reduced substantially by reducing the supply current and the supply voltage (down to 5 V or even below), or by applying the simple cascode buffer used in [1].

III. Experimental Results

The chips were fabricated in a commercial 0.35 μm SiGe production technology (Infineon's B7HF [4], also used in [1]) as part of a multiproject wafer. In this run, the transit frequency f_T of the transistors was decreased to 62 GHz, but their maximum oscillation frequency $f_{\max}$ was increased to about 90 GHz at $V_{CE} = 1$ V, compared to the data sheet values (72 GHz and 75 GHz, respectively). This might be mainly a consequence of the reduced doping concentration in the (selectively implanted) collector, which increases the breakdown voltage. Four Cu metallization layers were available. The size of this multipurpose chip is 0.89 mm $\times$ 1.3 mm and is mainly given by the pads and by the microstrip lines for the lower frequency ranges. Chip photos with the characteristic, adjustable microstrip lines look similar to that presented in [1].

The performance of the VCOs was measured by use of a 50-GHz spectrum analyzer (Agilent 8565E). For frequencies above 50 GHz, a mixer for down conversion is required (Agilent 11 970V).[2] The circuits were measured on-wafer, using a 110-GHz GSGSG probe, and also mounted on a simple (non-optimized) measurement socket with microstrip lines and coaxial connectors. A similar socket has also been used in [1], but now the K-connectors are replaced by V-connectors which are specified up to 65 GHz. Conventional wire bonding was applied.

Fig. 2 shows the measured oscillation frequency (f_{osc}) and single-sideband (SSB) phase noise at 1 MHz offset frequency in dependence on the bias voltage V_B (see Fig. 1). Apart from the dashed lines in the upper plots of Fig. 2, the results are related to a mounted chip with output buffer. The three frequency ranges were adjusted by cutting interconnection lines on the chip. The plots at the top of Fig. 2 represent the highest frequency range

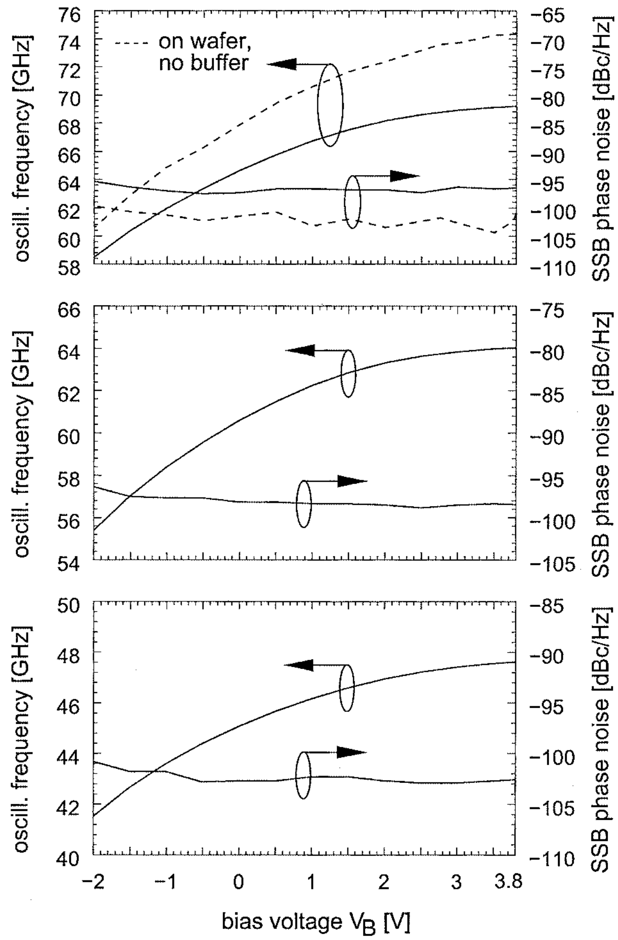

Fig. 2. Oscillation frequency and SSB phase noise (at 1 MHz offset frequency) in dependence on bias voltage V_B for three arbitrarily chosen frequency ranges. Apart from the dashed lines (top), the results are related to a mounted chip with output buffer.

achieved. It is overlapped by the middle plots with a center frequency of about 60 GHz. The lower plots demonstrate that even the frequency range required for 40 and 80 Gb/s ETDM systems can be adjusted on the same chip. It should be noted that also the gaps between the frequency ranges in Fig. 2 can be covered by cutting the corresponding interconnection lines. In all cases, a wide tuning range without any spurious oscillations is observed, which is maximal for the upper frequency range (since there the constant capacitance ΔC_E is eliminated). The phase noise is quite low compared to other millimeter-wave VCOs with wide tuning range and low enough for the intended applications. In the upper frequency range (top of Fig. 2) an average value of -96.5 dBc/Hz and in the lower range (bottom of Fig. 2) of -102.5 dBc/Hz was measured at 1 MHz offset frequency.[3] For comparison with other publications on millimeter-wave oscillators, the results of an on-wafer measurement for a design without output buffer are shown in Fig. 2 for the highest frequency range (dashed lines). Now, the maximum oscillation frequency is increased to 74 GHz. The phase noise averaged over the total frequency range is decreased to -102 dBc/Hz and the phase noise around 74 GHz is -104 dBc/Hz only. The phase

[1]Applying one of today's SiGe preproduction technologies (standing out for much higher f_T and $f_{\max}$) gain and output power can be significantly increased.

[2]The output power measured by use of this (calibrated) V-Band mixer agree quite well with power-meter measurements, performed by other groups.

[3]Phase noise measurements with a special equipment showed even lower values (by about -1 dBc/Hz).

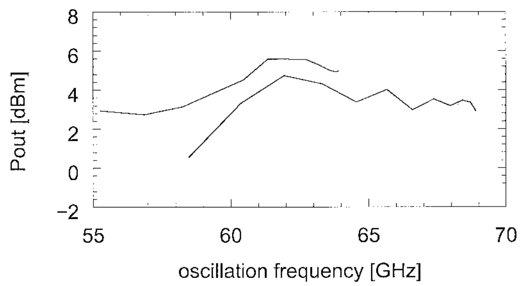

Fig. 3. Single-ended output power ($P_{\rm out}$) of a mounted VCO chip with output buffer in dependence on oscillation frequency for the two upper frequency ranges in Fig. 2.

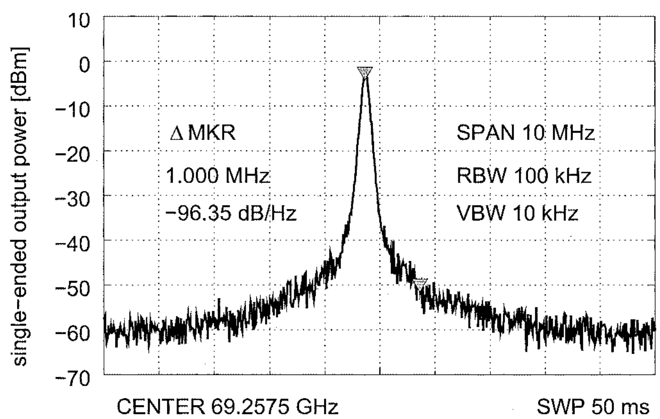

Fig. 4. Spectrum of the single-ended output power of of a mounted chip with output buffer at a center frequency of about 69 GHz. Due to the losses in the measurement set-up, the factual output power is higher (cf. Fig. 3).

noise improvement, compared to the mounted chip with output buffer, is mainly a result of the direct measurement of the oscillator-core output by RF probes, as also observed in [1].

Fig. 3 shows the single-ended output power of a mounted VCO with output buffer for the two upper frequency ranges in Fig. 2. (For the differential output, the output power is 3 dB higher.) In these plots, the losses by the measurement set-up have been taken into account. Higher output power was measured for a VCO without output buffer. As an example, an on-wafer measurement at 69 GHz showed an improvement by 3.5 dBm compared to Fig. 3.[4]

Finally, Fig. 4 shows the spectrum of the singled-ended output power at the maximum oscillation frequency of about 69 GHz for a mounted VCO chip with output buffer.

[4]In this case, the current through the oscillator core was increased by 13 mA.

The results presented have been measured at a temperature of the measurement socket of 30 °C. A numerical example shall give a feeling for the VCOs temperature dependence: At a medium frequency of 62 GHz and an increase of the socket temperature from 15 °C to 55 °C, the output power decreases by 1.3 dBm and the oscillation frequency by 350 MHz, while the change of phase noise remains less than 0.5 dBc/Hz.

Besides the output buffer in Fig. 1, also a simple modified cascode buffer stage has been used (see remarks at the end of Section II in [1]). Simulations and measurements show similar phase noise at somewhat increased output power and reduced power consumption. However, the supply voltage has to be increased to −6.5 V and the decoupling capability is less perfect (but is sufficient for most applications).

IV. Conclusions

It has been demonstrated that VCOs operating up to around 70 GHz can be fully integrated in a commercial SiGe production technology with moderate f_T and $f_{\rm max}$. Despite the wide tuning range of about 15% of the oscillation frequency, reasonably low values of the phase noise were obtained. Based on the results presented and on careful simulations, it is expected that low-cost VCOs for 77 GHz automotive radar systems with powerful output buffer can be realized in one of today's SiGe preproduction technologies with their much higher transistor cut-off frequencies f_T and $f_{\rm max}$.

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